Claims:

1. A discrete testing apparatus for testing a semiconductor integrated circuit device in die form, comprising:

a) a first plate;

b) a die-receiving cavity in the first plate;

c) a second plate associated with the first plate;

d) one of the first and second plates having a plurality of connector terminals thereon;

e) a die attachment surface located within the die receiving cavity, the die attachment surface having a plurality of circuit traces extending therefrom, the circuit traces extending to contacts to establish electrical communication with contact locations on the die;

f) the plurality of contacts being positioned so that, when the die is positioned in the die-receiving cavity, the contacts are in alignment with contact locations on the die and extending to the contact locations;

g) the plurality of contacts being formed with at least one raised portion, the raised portion extending sufficiently that it may penetrate its respective contact location on the die, thereby establishing electrical communication with said contact location, said extension of the raised portion being limited so that, when a force is applied to the raised portion is significantly less than a force required for portions of the contacts outside of the raised portion to penetrate its respective contact location, thereby limiting a penetration depth of the bump contacts at the contact location; and

h) the connector terminals in electrical communication with the contacts, the connector terminals being mounted to the one of said plates.

2. A discrete testing apparatus as described in claim 1, further comprising:

said one raised portion extending so as to penetrate to less than 2/3 of a thickness of its respective contact location on the die.

3. A discrete testing apparatus as described in claim 1, further comprising:

said one raised portion extending so as to penetrate to less than 1/2 of a thickness of its respective contact location on the die.

4. A discrete testing apparatus as described in claim 1, further comprising:

said one raised portion extending so as to penetrate to less than 2/3 of a thickness of its respective contact location on the die and said one raised portion extending at least 5000Å.

5. A discrete testing apparatus as described in claim 1, further comprising:

the die attachment surface being formed of semiconductor material, and the circuit traces being formed on the semiconductor material by semiconductor circuit fabrication techniques.

6. A discrete testing apparatus as described in claim 5, further comprising:

the die attachment surface being of a thickness sufficient to be substantially rigid.

7. A discrete testing apparatus as described in claim 5, further comprising:

the die attachment surface being sufficiently thin to be partially flexible.

8. A discrete testing apparatus as described in claim 5, further comprising:

the die attachment surface being formed of a structure which includes silicon material, and the circuit traces being formed on the silicon material by semiconductor fabrication techniques.

9. A discrete testing apparatus as described in claim 8, further comprising:

the die attachment surface being of a thickness sufficient to be substantially rigid.

10. A discrete testing apparatus as described in claim 8, further comprising:

the die attachment surface being sufficiently thin to be partially flexible.

11. A discrete testing apparatus as described in claim 1, further comprising:

a) the die attachment surface being formed of a ceramic insulator, and the circuit traces being formed on a surface of the substrate; and

b) the die attachment surface having said plurality of circuit traces formed thereon extending from the contacts to

connection points on said one of the first and second plates having a plurality of contacts thereon.

12. A discrete testing apparatus as described in claim 1, further comprising:

a) the die attachment surface being formed of a ceramic insulator, and the circuit traces being formed on a surface of the substrate;

b) the die attachment surface having said plurality of circuit traces formed thereon extending from the contacts to connection points on said one of the first and second plates having a plurality of contacts thereon; and

c) the die attachment surface being sufficiently thin to be partially flexible.

13. A discrete testing apparatus as described in claim 1, further comprising:

the die attachment surface being positioned in the die receiving cavity so that the plurality of contacts on the die attachment surface face away from the first plate, wherein the die is positioned above the die attachment surface with the contact locations on the die facing the die receiving cavity.

14. A discrete testing apparatus as described in claim 1, further comprising:

the die attachment surface being positioned in the die receiving cavity so that the plurality of contacts on the die attachment surface face are in a face up position with respect to the die receiving cavity and the die is positioned above the die attachment surface with the contact locations in a face down position on the die facing the die receiving cavity.

15. A discrete testing apparatus as described in claim 1, further comprising:

the die being positioned in the die receiving cavity so that the contact locations on the die are in a face up position with respect to the plurality of contacts on the die attachment surface and the die attachment surface is positioned above the die with the plurality of contacts in a face down position on the die attachment surface the die receiving cavity.

16. A discrete testing apparatus as described in claim 1, further comprising:

a pad which is electrically conductive in a Z-axis, normal to a plane of the pad, and which provides electrical isolation across the plane of the pad, the pad being positioned between the die and the plurality of contacts.

17. A discrete testing apparatus as described in claim 1, further comprising:

a) a resilient pad to bias die received in the die receiving cavity with the contacts after the first and second plates have been mated, to apply sufficient pressure to maintain ohmic contact between said substrate and said contact locations on the die; and

b) said contacts cooperating with said pad to apply sufficient pressure between said pad and said contact locations on the die to establish ohmic contact with said contact locations on the die.

18. A discrete testing apparatus as described in claim 1, further comprising:

an elastomeric strip further securing the substrate in a position within the die receiving cavity by means of electrostatic attraction and frictional forces, thereby permitting the substrate to be maintained in a positional alignment with respect to the die receiving cavity after being

placed into the die receiving cavity and prior to mating the second plate with the first plate.

19. A discrete testing apparatus as described in claim 1, further comprising:

an elastomeric strip further securing the die in a position within the die receiving cavity by means of electrostatic attraction and frictional forces, thereby permitting the die to be maintained in a positional alignment with respect to the die receiving cavity after being placed into the die receiving cavity and prior to mating the second plate with the first plate.

20. A discrete testing apparatus as described in claim 1, further comprising:

a) first and second plates biasing the die toward the die attachment surface in order to establish said electrical communication of the contacts with the contact locations on the die;

b) the second plate being secured to the first plate by a clamp, the clamp applying biasing pressure for said biasing of the die toward the die attachment surface; and

c) said contacts cooperating with said first and second plates and said clamp to apply sufficient pressure between said pad and said contact locations on the die to establish ohmic contact with said contact locations on the die.

21. A discrete testing apparatus for testing a semiconductor device in die form, comprising:

a) a first plate;

b) a die-receiving cavity in the first plate;

c) a second plate;

d) means to secure the first and second plates together;

e) an die attachment surface having a plurality of conductors thereon and dimensioned so as to fit within the

testing apparatus adjacent to the die when the die is in the die receiving cavity;

f) a pad which is electrically conductive in a Z-axis, normal to a plane of the pad, and which provides electrical isolation across the plane of the pad, the pad being positioned over the die between the die and the plurality of die attachment surface; and

g) a plurality of contacts on the plurality of conductors, the contacts being positioned so that, when the first plate and the second plate are aligned by the alignment means and the die and the die attachment surface are positioned in the die-receiving cavity, the contacts are in alignment with contact locations on the die;

h) connector terminals in an electrical communication with the plurality of contacts; and

i) a support to hold the die, the pad, and the die attachment surface together when the first plate and the second plate are secured together, wherein

when the first and second plates are secured together with the die in the die receiving cavity, a plurality of said contact locations are in electrical communication with the connector terminals, and the plurality of contacts result in the Z-axis conductive pad causing a portion of the pad to establish ohmic contact with said contact locations, said contacts being formed so that, when a force is applied to the contact is significantly less than a force which would cause the Z-axis conductive pad to significantly damage the contact location at locations where said ohmic contact is not established.

22. A discrete testing apparatus as described in claim 21, further comprising:

the die attachment surface being formed of a structure which includes silicon material, and the circuit traces being formed on the silicon material by semiconductor fabrication techniques.

23. A discrete testing apparatus as described in claim 22, further comprising:

the die attachment surface being of a thickness sufficient to be substantially rigid.

24. A discrete testing apparatus as described in claim 22, further comprising:

the die attachment surface being sufficiently thin to be partially flexible.

25. A discrete testing apparatus as described in claim 21, further comprising:

a) the die attachment surface being formed of a ceramic insulator, and the circuit traces being formed on a surface of the substrate; and

b) the die attachment surface having said plurality of circuit traces formed thereon extending from the contacts to

connection points on said one of the first and second plates having a plurality of contacts thereon.

26. A discrete testing apparatus as described in claim 21, further comprising:

the die attachment surface extending beyond the confines of a fixture formed by the first and second plates and terminating in an external connector, the external connector including said connector terminals.

27. A discrete testing apparatus as described in claim 21, further comprising:

means, separate from said pad, to bias the die received in the die receiving cavity with the die attachment surface after the first and second plates have been mated, the means to bias cooperating with said pad to apply sufficient pressure between said pad and said contact locations on the die to establish ohmic contact between said pad and said contact locations on the die.

28. A discrete testing apparatus as described in claim 27, further comprising:

the means to bias comprising an elastomeric polymer.

29. A discrete testing apparatus for testing a semiconductor device in die form, comprising:

a) a first plate;

b) a die-receiving cavity in the first plate;

c) a second plate;

d) means to secure the first and second plates together;

e) an die attachment surface having a plurality of conductors thereon and dimensioned so as to fit within the testing apparatus adjacent to the die when the die is in the die receiving cavity;

f) a pad which is electrically conductive in a Z-axis, normal to a plane of the pad, and which provides electrical isolation across the plane of the pad, the pad being positioned over the die between the die and the plurality of die attachment surface; and

g) a plurality of contacts on the plurality of conductors, and formed with at least one raised portion, the contacts being positioned so that, when the first plate and the second plate are aligned by the alignment means and the die and the die attachment surface are positioned in the die-receiving cavity, the contacts are in alignment with contact locations on the die;

h) connector terminals in an electrical communication with the plurality of contacts; and

i) a support to hold the die, the pad, and the die attachment surface together when the first plate and the second plate are secured together, wherein

when the first and second plates are secured together with the die in the die receiving cavity, a plurality of said contact locations are in electrical communication with the

connector terminals, and the raised portions on the plurality of contacts resulting in the Z-axis conductive pad causing a portion of the pad to establish ohmic contact with said contact locations, said extension of the raised portion being limited so that, when a force is applied to the raised portion is significantly less than a force which would cause the Z-axis conductive pad to significantly damage the contact location at locations where said ohmic contact is not established.

30. A discrete testing apparatus as described in claim 21, further comprising:

the die attachment surface being formed of a structure which includes silicon material, and the circuit traces being formed on the silicon material by semiconductor fabrication techniques.

31. A discrete testing apparatus as described in claim 30, further comprising:

the die attachment surface being of a thickness sufficient to be substantially rigid.

32. A discrete testing apparatus as described in claim 30, further comprising:

the die attachment surface being sufficiently thin to be partially flexible.

33. A discrete testing apparatus as described in claim 21, further comprising:

a) the die attachment surface being formed of a ceramic insulator, and the circuit traces being formed on a surface of the substrate; and

b) the die attachment surface having said plurality of circuit traces formed thereon extending from the contacts to

connection points on said one of the first and second plates having a plurality of contacts thereon.

34. A discrete testing apparatus as described in claim 21, further comprising:

the die attachment surface extending beyond the confines of a fixture formed by the first and second plates and terminating in an external connector, the external connector including said connector terminals.

35. A discrete testing apparatus as described in claim 21, further comprising:

means, separate from said pad, to bias the die received in the die receiving cavity with the die attachment surface after the first and second plates have been mated, the means to bias cooperating with said pad to apply sufficient pressure between said pad and said contact locations on the die to establish ohmic contact between said pad and said contact locations on the die.

36. A discrete testing apparatus as described in claim 35, further comprising:

the means to bias comprising an elastomeric polymer.

37. A package for a semiconductor integrated circuit device in die form, comprising:

a) a housing

b) a substrate within said housing, the substrate having a plurality of circuit traces extending therefrom, the circuit traces extending to contacts to establish electrical communication with contact locations on the die, the circuit traces extending to contacts to establish electrical communication with contact locations on the die;

c) the plurality of contacts being formed with at least one raised portion, the raised portion extending sufficiently that it may penetrate its respective contact location on the die, thereby establishing electrical communication with said contact location, the plurality of contacts being formed with at least one raised portion, the raised portion extending

sufficiently that it may penetrate its respective contact location on the die, thereby establishing electrical communication with said contact location, said extension of the raised portion being limited so that, when a force is applied to the raised portion is significantly less than a force required for portions of the contacts outside of the raised portion to penetrate its respective contact location, thereby limiting a penetration depth at the contact location;

d) connector terminals in electrical communication with the contacts, the connector terminals extending from said housing; and

e) the connector terminals in electrical communication with the contacts.

38. A package as described in claim 37, further comprising:

a) the connector terminals being located on said substrate; and

b) said substrate extending beyond the confines of said housing.

39. A package as described in claim 37, further comprising:

a) the contacts being formed as raised asperities; and

b) the asperities being formed by doinking material which is deposited on the substrate.

40. A package as described in claim 37, further comprising:

a) the contacts formed as bumps on the substrate, with raised portions on the bumps; and

b) the raised portions being dimensioned such that they readily penetrate the contact locations on the die, while the remainder of the bump functions to limit penetration depth of the raised portion.

41. A package as described in claim 37, further comprising:

a pad which is electrically conductive in a Z-axis, normal to a plane of the pad, and which provides electrical isolation across the plane of the pad, the pad being

positioned between the die and the plurality of raised portions, wherein

the raised portions on the plurality of contacts result in the Z-axis conductive pad causing a portion of the pad to establish ohmic contact with said contact locations, said extension of the raised portion being limited so that, when a force is applied to the raised portion is significantly less than a force required to cause the Z-axis to damage the contact location at locations where said ohmic contact is not established.

42. A discrete testing apparatus as described in claim 1, further comprising:

said one raised portion from a level of a passivation layer on the semiconductor die to an extent sufficient to extend into its respective contact location on the die, wherein the penetration of the raised portion into the contact location on the die is controlled by the die attachment surface resting against the passivation layer.

43. A discrete testing apparatus as described in claim 1, further comprising:

said one raised portion from a level of a passivation layer on the semiconductor die to an extent sufficient to extend into its respective contact location on the die, wherein the penetration of the raised portion into the contact location on the die is controlled by the plurality of contacts resting against the passivation layer.

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